REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 3-14 are in this application. Claim 9 has been amended. Claims 1-2 have been cancelled. Claims 10-14 has been added to additionally claim the present invention. Claims 3-8 have been allowed.

The Examiner rejected claims 1 and 2 under 35 U.S.C. §103(a) as being unpatentable over Klein (U.S. Patent No. 4,205,330) in view of Takagi (U.S. Patent No. 4,003,071). As noted above, claims 1-2 have been cancelled. With respect to new claim 10, this claim recites:

> "a first transistor having:
> "a first semiconductor region;
> "spaced-apart first source and drain regions formed in the first semiconductor region;
> "a first channel located between the first source and drain regions, the first channel having a first channel length;
> "a layer of first gate oxide formed over the first channel; and
> "a gate formed over the layer of first gate oxide to contact the layer of first gate oxide, the gate being spaced apart from the first source and drain regions;
> "the first transistor conducting more than a leakage current when the gate, the first source, and the first semiconductor region are connected to a same potential;
> "a second transistor having:
> "a second semiconductor region, the second semiconductor region having a first conductivity type and a dopant concentration;
> "spaced-apart second source and drain regions of a second conductivity type formed in the second semiconductor region;
> "a second channel located between the second source and drain regions, the second channel having a second channel length, the first conductivity type, and a dopant concentration, no region of the first conductivity type with a dopant concentration substantially greater than the dopant concentration of the second semiconductor region lying between the second source and drain regions;

"a layer of second gate oxide formed over the second channel; and

"a gate formed over the layer of second gate oxide, the gate of the second transistor contacting the layer of second gate oxide;

"the second transistor being substantially non-conductive when the gate of the second transistor, the second source, and the second semiconductor region are connected to a same potential, the first channel length being shorter than the second channel length."

In rejecting prior claim 1, the Examiner pointed to the Klein reference as teaching all of the limitations of the claims, except for disclosing that the thickness of the first gate oxide is substantially less than the thickness of the second gate oxide. The Klein reference, however, fails to teach or suggest a first transistor that has a gate which is spaced apart from the source and drain regions as required by new claim 10.

For example, if the first source and drain regions of the first transistor of claim 10 are read to be n+ source and drain regions 37 and 38 shown in FIG. 4 of Klein, then the gate of the first transistor of claim 10 can not be read to be gate 34 shown in FIG. 4 of Klein because gate 34 is not spaced apart from the source and drain regions 37 and 38 as required by new claim 10, but instead directly contacts source region 37.

Thus, since the Klein reference fails to teach or suggest a first transistor with a gate as required by new claim 10, new claim 10 is patentable over Klein in view of Takagi. In addition, since claims 9 and 11-14 depend either directly or indirectly from claim 10, claims 9 and 11-14 are patentable over Klein in view of Takagi for the same reasons as claim 10.

Thus, for the foregoing reasons, it is submitted that the application is in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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